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10/777,097	02/13/2004	Jae-jun Moon	Q77183	4555

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EXAMINER	
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ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
11/23/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/777,097	MOON ET AL.	
	Examiner	Art Unit	
	Jeffrey S. Zweizig	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-9,11 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-9,11 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Drawing Objections

The scales in Figs. 10A-10C are small and illegible. Some labels are obscured. Some labels are not English. Correction is required.

Figs. 10A and 10B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

There appears to be no antecedent basis for the start up circuit means recited in claim 11. Perhaps "means prevent" should be --part prevents--. Also, "claims in claim 1" should be --claimed in claim 1--.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5, 7, 9 and 11 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art Fig. 1 in view of Wu et al. (5,307,007) and Lee (6,356,139).

Applicant's Prior Art Fig. 1 shows an output terminal node N12, a common node N11, a power source voltage Vcc, a grounded power source Vss, a first PMOS transistor MP11, a second PMOS transistor MP12, a first NMOS transistor MN13, a second NMOS transistor MN14 and a resistor R11 all connected as recited in claim 1.

Applicant's Prior Art Fig. 1 does not show a start-up capacitor as recited in claim 1, however, Applicant's Background of the Invention notes that start-up circuits are typically required with bias circuits such as that shown in Fig. 1. Furthermore, the body of cited Prior Art supports the notion that such bias circuits typically require start-up circuits.

Wu et al. Fig. 1 shows a similar bias circuit wherein components M1, M2, M3 and M4 are analogous to components MP11, MP12, MN13 and MN14, respectively. Further shown is a star-up capacitor C1 as recited in claim 1. It would have been obvious to one of ordinary skill in the art at the time of the invention to connect a capacitor as taught by Wu et al. between the output terminal node N12 and the common node N11 for the benefit of ensuring that the bias circuit properly starts. Moreover, all the claimed elements were known in the Prior Art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Applicant's Prior Art Fig. 1 does not specify a body connection as recited near the end of claim 1. Those of ordinary skill plainly understand that body connections are often schematically omitted for the sake of an uncluttered presentation. Where no body connection is shown, one conventionally assumes that the body is connected to the source because such a connection is the simplest, most straight forward way of terminating the body. Lee Fig. 1 shows a similar bias circuit wherein components P1, P2, N1, N2 and R1 are analogous to components MP11, MP12, MN13, MN14 and R11, respectively. Lee specifically shows that all the transistor bodies are connected to each of their respective sources. It would have been obvious to one of ordinary skill in the art at the time of the invention to connect the bodies of the transistors to their respective sources for the benefit of terminating the bodies. Applicant's lack of a specific implementation invites the combination. This body connection scheme is further

supported by Fig. 8 as shown in Applicant's IDS reference 2002-237186. All the claimed elements were known in the Prior Art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Claim 1 is amended to recite that the start up part is for improving stability characteristics at high frequencies. Little weight is given to this limitation since there is no claimed point of reference from which any improvement could be judged. Nevertheless, the limitation appears to be directed toward paragraph [51] of the specification, which describes stability improvements gained from the disclosed structure of the invention. Since Examiner's combination duplicates the disclosed structure, Examiner's combination would exhibit the same stability improvements.

Claim 1 is also amended to recite that noise from the power source voltage is eliminated. This limitation appears to be directed toward the absence of circuit 20 as shown in Applicant's Prior Art Fig. 2 (paragraph [09]). Examiner's combination does not include any element resembling circuit 20. Moreover, Examiner's combination duplicates the disclosed structure. Since Examiner's combination duplicates the disclosed structure, Examiner's combination would exhibit the same noise eliminating characteristics.

Claim 1 is obvious.

The output node outputs a constant bias voltage as recited in claim 5. Claim 5 is obvious.

Bias circuits exist for the very purpose of providing bias to another circuit outside the bias circuit. Claim 7 is obvious.

There is no patentable difference seen between an "output terminal node" and an "output node". Claim 9 is otherwise identical to claim 1 and is obvious for the same reasons noted above.

Claim 11 appears to be directed toward paragraph [02] of the specification, which indicates that bias circuits without start up circuits may be subject to transient states. But since Examiner's combination does include a start up circuit, Examiner's combination would prevent transient states as recited in claim 11. Moreover, Examiner's combination duplicates the disclosed structure. Thus, Examiner's combination would exhibit the same transient state prevention characteristics.

Claims 3, 6 and 8 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art Fig. 1 in view of Wu et al. (5,307,007) and Park et al. (5,880,625).

Applicant's Prior Art Fig. 1 shows an output terminal node N12, a second common node N11, a power source voltage Vcc, a grounded power source Vss, a third PMOS transistor MP11, a fourth PMOS transistor MP12, a first NMOS transistor MN13, a second NMOS transistor MN14 and a resistor R11 all connected as recited in claim 3.

Applicant's Prior Art Fig. 1 does not show a second capacitor as recited in claim 3. Wu et al. Fig. 1 shows a second capacitor C1 as recited in claim 3. In would have been obvious to combine these elements as noted above.

Applicant's Prior Art Fig. 1 does not show the first and second PMOS transistors as recited in claim 3, however, such cascode circuit arrangements are well know as shown by the body of cited Prior Art. Park et al. Fig. 5 shows a specific example of a cascode bias circuit wherein components M56, M55, M52, M51 and R are analogous to components MP11, MP12, MN13, MN14 and R11, respectively. Park et al. shows additional cascode components in the form of a first PMOS transistor M54 and a second PMOS transistor M53. It would have been obvious to one of ordinary skill in the art at the time of the invention to augment Applicant's Prior Art Fig. 1 with cascode components M54 and M53 as taught by Park et al. for the benefit of, for example, reducing current fluctuations due to channel length modulation effects (col 4 ln 20). According to Examiner's combination, the junction of the gates of M54 and M53 form the claimed first common node. All the claimed elements were known in the Prior Art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

The Wu et al. reference also considers cascode circuit arrangements. Fig. 3, for example, shows common nodes and output nodes at the gate junctions of transistors M3/M4, M5/M6 and M7/M8 with a capacitor connected between each pair of junctions. It would have been obvious to one of ordinary skill in the art at the time of the invention to connect a first capacitor as taught by Wu et al. between the first common node and the second common node and to connect a second capacitor as taught by Wu et al. between the second common node and the output node for the benefit of ensuring that

the bias circuit properly starts. Moreover, all the claimed elements were known in the Prior Art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Claim 3 is amended to recite that the start up part is for improving stability characteristics at high frequencies. Little weight is given to this limitation since there is no claimed point of reference from which any improvement could be judged. Nevertheless, the limitation appears to be directed toward paragraph [51] of the specification, which describes stability improvements gained from the disclosed structure of the invention. Since Examiner's combination duplicates the disclosed structure, Examiner's combination would exhibit the same stability improvements.

Claim 3 is also amended to recite that noise from the power source voltage is eliminated. This limitation appears to be directed toward the absence of circuit 20 as shown in Applicant's Prior Art Fig. 2 (paragraph [09]). Examiner's combination does not include any element resembling circuit 20. Moreover, Examiner's combination duplicates the disclosed structure. Since Examiner's combination duplicates the disclosed structure, Examiner's combination would exhibit the same noise eliminating characteristics.

Claim 3 is obvious.

The output node outputs a constant bias voltage as recited in claim 6. Claim 6 is obvious.

Bias circuits exist for the very purpose of providing bias to another circuit outside the bias circuit. Claim 8 is obvious.

New claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Floyd (6,198,312) in view of Wu et al. (5,307,007).

Floyd Fig. 4 shows a cascode bias circuit part 22 comprising a power source voltage VDD, a grounded power source 36, a first PMOS transistor 30, a second PMOS transistor 26, a first common node (gate of 26), a resistor 24, a first NMOS transistor 58, a second NMOS transistor 56, a second common node (gate of 56), a third NMOS transistor 32, a fourth NMOS transistor 28, an output node 68 and grounded body connections for the first 58 and second 56 NMOS transistors, all connected and arranged as recited in claim 14. Fig. 4 further shows start up circuit part 62/64/66 as opposed to the two-capacitor start up circuit part recited in claim 14.

The Wu et al. reference also considers cascode bias circuit part arrangements. Fig. 3, for example, shows common nodes and output nodes at the gate junctions of transistors M3/M4, M5/M6 and M7/M8 with a capacitor connected between each pair of junctions. It would have been obvious to one of ordinary skill in the art at the time of the invention to connect a first capacitor as taught by Wu et al. between the first common node and the second common node of Floyd and to connect a second capacitor as taught by Wu et al. between the second common node and the output node of Floyd. This combination has the advantage of replacing the multi-transistor start up circuit part 62/64/66 with a simple two-capacitor start up circuit part.

Moreover, all the claimed elements were known in the Prior Art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Claim 14 is obvious.

Alternately, new claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art Fig. 1 in view of Wu et al. (5,307,007), Park et al. (5,880,625) and Floyd (6,198,312).

New claim 14 is merely the complementary embodiment of that recited in previously rejected claim 3. For example, claim 3 is directed toward Applicant's Fig. 13 whereas new claim 14 is directed toward Applicant's Fig. 14. Fig. 14 is simply the complement of Fig. 13. As pointed out above, claim 3 is unpatentable over Applicant's Prior Art Fig. 1 in view of Wu et al. and Park et al. Floyd Figs. 3 and 6 teach that bias circuit parts have complementary embodiments. One or the other is implemented depending on the needs of the downstream circuitry. In fact, Fig. 4 shows the complementary arrangement of Examiner's combination as applied to claim 3. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a complementary embodiment of Examiner's claim 3 combination. All the claimed elements were known in the Prior Art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one

of ordinary skill in the art at the time of the invention. Applicant's Prior Art Fig. 1, Wu et al. and Park et al. do not show body connections, but as pointed out above, Floyd Fig. 4 shows that NMOS body connections may be made to ground.

Moreover, the Prior Art of record is replete with other examples of bias circuits along with equivalent complementary embodiments. See for example, Kim (6,184,745) Figs. 1 and 4 and Yamazaki (5,180,967) Figs. 1 and 2.

Claim 14 is obvious.

Response to Amendments and Arguments

The rejections have been revised to reflect the amendments to the claims.

Regarding Applicant's arguments, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See MPEP 2145 section II for further discussion.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey S. Zweizig whose telephone number is (571) 272-1758. The examiner can normally be reached on Monday thru Wednesday 6:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571) 272-1988. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeffrey S. Zweizig/
Primary Examiner, Art Unit 2816

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